

Application No. 10/065,446  
Docket No. DP-307128  
Amendment dated June 21, 2004  
Reply to Office Action of March 19, 2004

**Amendments to the Specification:**

Please replace paragraph [0011] with the following amended paragraph:

**[0011]** Figure 1 represents an optical sensor package 10 that can be fabricated and surface mounted in accordance with this invention. The package 10 is shown as being formed by solder bonding a device chip carrier 12 to a capping chip 14, such that an optical sensing device chip 16 is enclosed and protected within a cavity 18 defined by and between the capping chip 14 and the device chip carrier 12, e.g., the cavity 18 is formed by a recess 20 in the device chip carrier 12. While shown as being a stack of an individual capping chip 14 and chip carrier 12, the invention preferably entails the use of wafers that are bonded together and later singulated to form any desired number of packages 10 of the type shown in Figure 1. With this approach, a device chip carrier wafer is processed to have an array of recesses 20, each of which will form a cavity 18 with a capping wafer to contain an optical sensing device chip 16.

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Please replace paragraph [0013] with the following amended paragraph:

[0013] The device chip carrier 12 is preferably formed of low temperature co-fired ceramic (LTCC), though essentially any technology capable of providing low-resistance electrical paths (e.g., metal vias 28, discussed below) through the chip carrier 12 could be used. A preferred LTCC material is referred to as 951 Low-Temperature Cofire Dielectric Tape, available from DuPont, though other LTCC materials could be used. An advantage of forming the chip carrier 12 of an LTCC material is that the vias 28 and recess 20 in the device chip carrier 12 can be fabricated during the green tape portion of LTCC fabrication and then fired. A suitable process for forming the vias 28 in an LTCC material involves a screen printing technique well known in the art, and therefore will not be described here in any detail. Alternatively, the vias 28 and recess 20 would require being formed by machining, etching and/or additional process steps if another material for the device chip carrier 12 is used.

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Please replace paragraph [0014] with the following amended paragraph:

**[0014]** The optical sensing device chip 16 is represented as being a flip chip comprising a semiconductor substrate 30. An optical sensing element (not shown) is located on the upper surface of the chip 16, and can have a variety of transduction configurations. In a preferred embodiment, the sensing element is an infrared-sensing thermopile configured and fabricated in accordance with U.S. Patent Application Serial Nos. 10/065,447 and 10/065,448, ~~{Attorney Docket Nos. DP-306616 and DP-307129}~~, incorporated herein by reference. Signal conditioning circuitry (not shown) for the optical sensing element can be formed on the chip 16, though it is foreseeable that the circuitry could be formed on a separate signal conditioning chip that is electrically connected to the sensing device chip 16 through the device chip carrier 12.

Please replace the paragraph in the Abstract of the Disclosure with the amended paragraph submitted herewith on a separate sheet pursuant to 37 CFR 1.72.